Amendments to the Claims

Please amend the claims such that the results are:

1. (Currently amended) An integrated circuit for processing events related to communication packets, said integrated circuit comprising:

a core processor configured to execute software to process a series of communication packets, the processing of each packet being an event and having associated data and context information; and

a co-processor comprising a plurality of state information buffers for storing state information, a plurality of context buffers for storing context information associated with a plurality of events and a plurality of data buffers for storing data associated with the plurality of events where the state information comprises a data buffer pointer pointing to one of the plurality of data buffers and a context buffer pointer pointing to one of the plurality of context buffers, where the plurality of state information buffers, the plurality of context buffers and the plurality of data buffers are formed as special purpose dedicated hardware buffers in the integrated circuit;

the state information is associated with events wherein each of said state information buffers has an in-use counter indicating the number of events associated with the contents of said buffer.

2. (Canceled)

3. (Previously amended) The integrated circuit of claim 1 wherein said co-processor comprises an in-use counter associated with each of said context buffers.

4. (Canceled)

5. (Previously amended) The integrated circuit of claim 1 wherein said co-processor comprises an in-use counter associated with each of said data buffers.

6. (Previously amended) The integrated circuit of claim 1 wherein said plurality of data buffers each having an in-use counter whereby data can be transferred from one event to another event by changing information in a data buffer.

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Currently amended) An integrated circuit for processing events related to communication packets, said integrated circuit comprising:

a core processor configured to execute software to process a series of communication packets, the processing of each packet being an event and having associated data and context information; and

a co-processor comprising a plurality of state information buffers for storing state information associated with events wherein each of said state information buffers having an in-use counter indicating the number of events associated with the contents of said buffer, wherein said co-processor comprises a plurality of data only information buffers, a plurality of context information buffers, an in-use counter for each of said data only buffers and an in-use counter for each of said context buffers where data can be passed from one event to another event by changing the data in one of said state information buffers and where the state information comprises a data only buffer pointer pointing to one of the plurality of data only information buffers and a context information buffer pointer pointing to one of the pluralities of context information buffers and where the plurality of state information buffers, the plurality of context buffers and the plurality of data buffers are formed as special purpose dedicated hardware buffers in the integrated circuit.

11. (Currently amended) A method of processing events related to communication packets in an integrated circuit which includes a core processor and a co-processor having a state information buffer for storing state information, a context buffer for storing context information and a data buffer for storing data where the state information comprises a data buffer pointer and a context pointer-where the data buffer pointer points to the data buffer and the context pointer points to the context buffer, the state information for an event is stored separate from the data associated with said event, said state information buffer having an associated in use counter and where the state information buffer, the context buffer and the data buffer are formed as special purpose dedicated hardware buffers in the integrated circuit, the method comprising:

incrementing the in-use counter associated with said state information buffer when an event is associated with said state information buffer; and

decrementing the in-use counter of said state information buffer when said event associated with said buffer is finished.

12. (Canceled)

13. ((Previously amended) The method of claim 11 wherein said integrated circuit comprises an in-use counter for said context information buffer and the method further comprises:

incrementing the in-use counter associated with said context buffer when an event is associated with said context buffer; and

decrementing the in-use counter of said context buffer when said events associated with said context buffer is finished.

14. (Canceled)

15. (Previously amended) The method of claim 11 wherein said integrated circuit comprises an in-use counter associated with said data buffer and the method further comprises:

incrementing the in-use counter associated with said data buffer when an event is associated with said data buffer; and

decrementing the in-use counter of said data buffer when said event associated with said data buffer is finished.

16. (Currently amended) An integrated circuit for processing events associated with communication packets which includes a core processor and a co-processor, the improvement which comprises, separate buffers for data, context, and state information and in-use counters for all of said buffers, whereby the contents of a data can be passed from one event to another event, each of said events having state information in a separate state information buffer where the state information comprises a data buffer pointer pointing to a data buffer, and a context pointer pointing to a context buffer and where the separate state information buffer, the separate context buffer and the separate data buffer are formed as special purpose dedicated hardware buffers in the integrated circuit.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Previously presented) The integrated circuit of claim 16 which includes a plurality of data buffers, a plurality of state information buffers and a plurality of context information buffers, each of said plurality of data buffers and each of said plurality of state information buffers and each of said plurality of context buffers having an in-use counter which is incremented when an event is associated with one of the plurality of data buffers or with one of the plurality of state information buffers or with one of said plurality of context buffers and decremented when an event is finished utilizing one of the plurality of data buffers or with one of the plurality of state information buffers or with one of said plurality of context buffer.

21. (Canceled)